What is claimed is:

1. A semiconductor device having a [CMOS] circuit comprising an n-channel [TFT] and a p-channel [TFT], said semiconductor device comprising:

each gate electrode of said n-channel TFT and said p-channel TFT has a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with both said first conductive layer and said gate insulating film;

a semiconductor layer of said n-channel TFT comprising a first channel formation region, a first impurity region being in contact with said first channel formation region, and a second impurity region being in contact with said first impurity region; and

a semiconductor layer of said p-channel TFT comprising a second channel formation region and a third impurity region being in contact with said second channel formation region,

wherein said first impurity region of said n-channel TFT is disposed so as to completely [overlaps] underlaps with said second conductive layer;

wherein said third impurity region of said p-channel TFT is disposed so as to partially [overlaps] underlaps with said second conductive layer.